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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/762,658	01/22/2004	Dean Z. Tsang	TSA-001XX	5151
207 7590 07/13/2007 WEINGARTEN, SCHURGIN, GAGNEBIN & LEOVICI LLP TEN POST OFFICE SQUARE BOSTON, MA 02109			EXAMINER PHAM, LONG	
			ART UNIT 2814	PAPER NUMBER
			MAIL DATE 07/13/2007	DELIVERY MODE PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.		Applicant(s)	
	10/762,658		TSANG, DEAN Z.	
	Examiner		Art Unit	
	Long Pham		2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 16 April 2007.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-35 is/are pending in the application.
- 4a) Of the above claim(s) 27-35 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-26 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date <u>04/16/07</u> | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

New grounds of rejection

Claim Rejections - 35 USC § 103

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claims 1-7 and 16-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Misewich et al. (US patent 6,365,913) in combination with Chu et al. (US publication 2004/0227154).

With respect to claims 1, 4, 5, Misewich et al. teach a transistor device comprising
(see claims 1-40 and associated figures):

a source;

a drain;

a gate;

a p-type hole metal channel (see fig. 1 and col. 6, lines 40-50) or channel layer, the channel is being positioned relative to the gate such that the carriers in the channel are controlled by the gate inherently;

Misewich et al. fail to teach the ranges for the thicknesses of the channel layer.

Chu et al. teach a MOS device in which the thickness of channel is between 1.5 to 2.0 nm . See [00501].

It would have been obvious to one of ordinary skill in the art of making semiconductor devices to use the range for the thickness of channel of Chu et al. in the device of Misewich et al. to achieve enhanced hole mobilities. See para [0050].

Further with respect to claim 1, it is submitted that the channel would inherently has carriers which are inherently controlled by the gate.

With respect to claim 3, Misewich et al. appear to fail to teach that substrate is made of silicon.

However, the use of silicon as substrate material is well-known in the art.

With respect to claim 2, Misewich et al. fail to teach that the channel is located between a gate insulator and an insulator.

However, the formation of a channel over a SOI substrate (including an insulator) and a gate insulator over the channel is well-known.

With respect to claims 6 and 7, Misewich et al. further teach that the transistor comprises of an enhancement or depletion mode device. See col. 1, lines 57-64.

With respect to claim 16, it is submitted that the channel would inherently have carriers which are inherently controlled by the gate.

With respect to claim 17, Misewich et al. further teach the source comprises a p-type metal and the drain comprises of a p-type metal and wherein the metal channel is a p-type metal (see fig. 1 and col. 6, lines 40-50). Further since Misewich et al. in combination with Chu et al. teach the claimed thickness for the metal channel, the carriers would inherently be controlled to form a p-channel depletion-mode device.

With respect to claim 18, Misewich et al. further teach the source comprises a n-type metal and the drain comprises of an p-type metal and wherein the metal channel is a p-type metal (see fig. 1 and col. 6, lines 40-50). Further since Misewich et al. in combination with Chu et al. teach the claimed device, an n-type inversion layer would inherently be formed on the p-type metal when a positive gate voltage is applied to form an n-channel enhancement mode device.

With respect to claim 19, Wisewich et al. further teach the device comprises of a CMOS device. See col. 6, lines 40-60.

With respect to claim 15, the formation of channel having plurality of layers is well-known.

With respect to claim 21, Wisewich et al. further teach the metal channel comprises of metal alloy. See col. 6, lines 40-50.

Claims 8, 9, 10, 11, 12, 13, 14, and 15 and 22-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wei et al. (US publication 2004/0169227) in combination with Misewich et al. (US patent 6,365,913), Chu et al. (US publication 2004/0227154), Song et al. (US patent 2004/0149579), and Ogura et al. (US publication 2002/0045319).

With respect to claim 8, Wei et al. teach a field effect transistor comprising (see figs. 1 and 2A-2B and associated text):

- a channel 33 over an insulator 30B;
- a source and a drain 52; and
- a gate 36 and a gate insulator 34 over the channel.

Wei et al. fail to teach that the channel is made of n-type metal **or doped metal**.

Misewich et al. teach n-type channel made of metal to attain high density memory device, See claims 1-40 and col. 5, lines 60-62 and co. 6, lines 44-50.

It would have been obvious to one of ordinary skill in the art of making semiconductor devices to use n-type metal as channel material to obtain above advantage.

Further with respect to claim 8, Wei et al. further teach the source and drain include p-type material. See col. [0025].

Further with respect to claim 8, it is submitted that the channel would inherently have carriers which are inherently controlled by the gate.

With respect to claim 9, Wei et al. further teach the insulator further comprises an insulating layer 30B over a substrate 30A, the channel being positioned between the gate and the insulating layer and the gate insulator being positioned under the gate and over the channel.

With respect to claim 10, the use of silicon as substrate material is well-known.

With respect to claims 11 and 25, Wei et al. fail to teach the range for the thickness of the channel layer.

Chu et al. teach a MOS device in which the thickness of channel is between 1.5 to 2.0 nm. See [0050].

Further with respect to claim 25, Since Wei et al. in combination with Chu et al. teach the claimed thickness of the channel layer, it is inherently greater than the thickness of the p-type inversion layer.

It would have been obvious to one of ordinary skill in the art of making semiconductor devices to use the range for the thickness of channel of Chu et al. in the device of Wei et al. to achieve enhanced hole mobilities. See [0050].

With respect to claim 12, Wei et al. further teach the device comprises of a CMOS device. See [0007].

With respect to claim 13, Wei et al. further teach an encapsulation layer 21. See fig. 1.

With respect to claim 14, Wei et al. fail to teach the range for the width of the channel.

Song et al. teach a channel having width of less than 500 nm. See claim 4.

It would have been obvious to one of ordinary skill in the art of making semiconductor devices to use the range for width of the channel of Song et al. in the device of Wei et al. to achieve the benefit of controlling current flow through the channel by controlling the voltage applied across the channel. See [0005].

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Further with respect to claim 14, Wei et al. fail to teach the range of the length of the channel.

Ogura et al. teach a channel having a length of 40 nm to reduce voltage and increase speed. See [0024].

It would have been obvious to one of ordinary skill in the art of making semiconductor devices to use the length of the channel of Ogura et al. in the device of Wei et al. to achieve above advantage.

With respect to claim 15, the formation of channel having plurality of layers is well-known.

With respect to claim 24, Wisewich et al. further teach the metal channel comprises of metal alloy. See col. 6, lines 40-50.

With respect to claims 22, 23, and 26, since Wei et al. in combination with Misewich et al., Song et al, and Ogura et al. teach the claimed device, a p-type inversion layer would inherently be formed on a side of the n-type metal when a negative gate voltage is applied to form an p-channel enhancement mode device.

Response to Arguments

Applicant's arguments filed 04/16/07 have been fully considered but they are not persuasive. See below.

In response to the applicant's arguments in the paragraphs on pages 8, 9, 10, and 11 of the amendment dated 04/16/07, it is submitted that the metal part of the channel of Misewich et al. would be inherently functioning as channel and the carriers in the channel would be inherently controlled by the gate. Further, it is submitted that present claims do not exclude the presence of other elements in the channel, that is the oxide part of the channel of Misewich et al.

In response to the applicant's arguments in the paragraphs on pages 8, 9, 10, and 11 of the amendment dated 04/16/07, it is submitted that Wei et al. in

combination with Misewich et al., Chu et al, Song, and Ogura teach the claimed invention as **presently written**.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Long Pham whose telephone number is 571-272-1714. The examiner can normally be reached on Mon-Frid, 10am to 5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on 571-272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Long Pham
Primary Examiner
Art Unit 2814

LP